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L9	21	equal ADJ4 number ADJ4 pulses ADJ4 (output or outputting) first second	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/12/12 09:50

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L11	100335	computer readable medium	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/12/12 10:01
L12	88015	computer ADJ2 readable ADJ2 medium	USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	WITH	ON	2005/12/12 10:33
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1 The predecessor attack: An analysis of a threat to anonymous communications systems
Matthew K. Wright, Micah Adler, Brian Neil Levine, Clay Shields
November 2004 **ACM Transactions on Information and System Security (TISSEC)**, Volume 7 Issue 4
Publisher: ACM Press
Full text available: pdf(295.25 KB) Additional Information: full citation, abstract, references, index terms

There have been a number of protocols proposed for anonymous network communication. In this paper, we investigate attacks by corrupt group members that degrade the anonymity of each protocol over time. We prove that when a particular initiator continues communication with a particular responder across path reformations, existing protocols are subject to the attack. We use this result to place an upper bound on how long existing protocols, including Crowds, Onion Routing, Hordes, Web Mixes, and D ...

Keywords: Privacy, anonymity, anonymous communication, predecessor attack

2 Low-power circuit techniques: An 8.3GHz dual supply/threshold optimized 32b integer ALU-register file loop in 90nm CMOS
Steven K. Hsu, Amit Agarwal, Kaushik Roy, Ram K. Krishnamurthy, Shekhar Borkar
August 2005 **Proceedings of the 2005 international symposium on Low power electronics and design ISLPED '05**
Publisher: ACM Press
Full text available: pdf(634.54 KB) Additional Information: full citation, abstract, references, index terms

In high performance microprocessors, integer execution cores are one of the hottest thermal spots and peak current/power delivery limiters. This paper describes a dual-supply and dual-threshold optimized 32-bit integer execution ALU and register file loop for 8.3GHz operation in 1.2V, 90nm CMOS technology. Aggressive supply/threshold scaling on the ALU and nominal supply/threshold on the register file enables up to 25% peak energy reduction without sacrificing performance or array bit-cells stab ...

Keywords: dual-Vt/Vcc, flip-flop, hot spot, level converter

3 Variable supply-voltage scheme with 95%-efficiency DC-DC converter for MPEG-4 codec

Fuyuki Ichiba, Kojiro Suzuki, Shinji Mita, Tadahiro Kuroda, Tohru Furuyama
August 1999 **Proceedings of the 1999 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(640.57 KB) Additional Information: full citation, references, citings, index terms

Keywords: DC-DC, PWM, low power, low voltage, variable supply voltage

4 Digital data processor for tracking the partially illuminated moon
H. James Wilcox
March 1964 **Communications of the ACM**, Volume 7 Issue 3
Publisher: ACM Press
Full text available: pdf(2.17 MB) Additional Information: full citation, abstract, references, index terms

A study of lunar tracking techniques and fabrication of a breadboard to assess the feasibility of the best technique selected was conducted to define a tracking system for observation of the sightline to the center of a partially illuminated moon. The data processing portion of the system is presented in detail and then described in general are the operation of the tracker head assembly for data readout, the operation of the entire system and the effect data processing considerations have o ...

5 Design methodology of ultra low-power MPEG4 codec core exploiting voltage scaling techniques
Kimiyoshi Usami, Mutsunori Igarashi, Takashi Ishikawa, Masahiro Kanazawa, Masafumi Takahashi, Mototsugu Hamada, Hideho Arakida, Toshihiro Terazawa, Tadahiro Kuroda
May 1998 **Proceedings of the 35th annual conference on Design automation**
Publisher: ACM Press
Full text available: pdf(289.77 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper describes a fully automated low-power design methodology in which three different voltage-scaling techniques are combined together. Supply voltage is scaled globally, selectively, and adaptively while keeping the performance. This methodology enabled us to design an MPEG4 codec core with 58% less power than the original in three week turn-around-time.

Keywords: MPEG4, codec, design automatian, flip-flops, level converters, low power, placement, synthesis, voltage scaling

6 Techniques and modules for element specification in a time - delay logic simulator
John L. Fike, S. A. Szygenda
June 1973 **Proceedings of the 1st symposium on Simulation of computer systems**
Publisher: IEEE Press
Full text available: pdf(872.73 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the development of element models (basic gates and flip-flops) for use in a multi-modal, assignable-delay logic simulator known as TEGAS2. The basic mechanism of this event-driven simulator is first described, together with the operation of the three basic simulation modes (nominal-delay two-value simulation, nominal-delay three-value simulation, and three-value simulation using an ambiguity region to provide race and hazard detection). The criteria used in d ...

7 Noise Figure Evaluation Using Low Cost BIST

Marcelo Negreiros, Luigi Carro, Altamiro A. Susin

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**

Publisher: IEEE Computer Society

Full text available: pdf(244.59 KB) Additional Information: full citation, abstract

A technique for evaluating noise figure suitable for BIST implementation is described. It is based on a low cost single-bit digitizer, which allows the simultaneous evaluation of noise figure in several test points of the analog circuit. The method is also able to benefit from SoC resources, like memory and processing power. Theoretical background and experimental results are presented in order to demonstrate the feasibility of the approach.

8 Verification of VHDL designs using VAL

Larry M. Augustin, Benoit A. Gennart, Youm Huh, David C. Luckham, Alec G. Stanculescu

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(737.10 KB) Additional Information: full citation, abstract, references, citings, index terms

VAL (VHDL Annotation Language) uses a small number of new language constructs to annotate VHDL hardware descriptions. VAL annotations, added to the VHDL entity declaration in the form of formal comments, express intended behavior common to all architectural bodies of the entity. Annotations are expressed as parallel processes that accept streams of input signals and generate constraints on output streams. VAL views signals as streams of values ordered by time. Generalized timing expressions ...

9 Power minimization in IC design: principles and applications

Massoud Pedram

January 1996 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 1 Issue 1

Publisher: ACM Press

Full text available: pdf(550.02 KB) Additional Information: full citation, abstract, references, citings, index terms

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift in which power dissipation is as important as performance and area. This article presents an in-depth survey of CAD methodologies and techniques for designing low power digital CMOS circuits and systems and describes the many issues facing designers at architectural, logical, and physical levels of design abstraction. It reviews some of the techniques and tool ...

Keywords: CMOS circuits, adiabatic circuits, computer-aided design of VLSI, dynamic power dissipation, energy-delay product, gated clocks, layout, low power layout, low power synthesis, lower-power design, power analysis and estimation, power management, power minimization and management, probabilistic analysis, silicon-on-insulator technology, statistical sampling, switched capacitance, switching activity, symbolic simulation, synthesis, system design

10 Efficient frequency domain video scrambling for content access control

Wenjun Zeng, Shawmin Lei

October 1999 **Proceedings of the seventh ACM international conference on Multimedia (Part 1)**

Publisher: ACM Press

Full text available: pdf(1.65 MB) Additional Information: full citation, abstract, references, index terms

Multimedia data security is very important for multimedia commerce on the Internet such as video-on-demand and real-time video multicast. Traditional cryptographic algorithms for data security are often not fast enough to process the vast amount of data generated by the multimedia applications to meet the real-time constraints. This paper presents a joint encryption and compression framework in which video data are scrambled efficiently in the frequency domain by employing selective bit scr ...

Keywords: compression, content access control, multimedia commerce, multimedia encryption, multimedia security, selective encryption, video scrambling

11 Self-adjusting output data compression: an efficient BIST technique for RAMs

V. N. Yarmolik, S. Hellebrand, H.-J. Wunderlich

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Publisher: IEEE Computer Society

Full text available: pdf(71.43 KB) Publisher Site

Additional Information: full citation, abstract, references, index terms

After write operations, BIST schemes for RAMS relying on signature analysis must compress the entire memory contents to update the reference signature. This paper introduces a new scheme for output data compression which avoids this overhead while retaining the benefits of signature analysis. The proposed technique is based on a new memory characteristic derived as the modulo-2 sum of all addresses pointing to non-zero cells. This characteristic can be adjusted concurrently with write operations ...

12 Electroid-oriented adiabatic switching circuits

David J. Frank, Paul M. Solomon

April 1995 **Proceedings of the 1995 international symposium on Low power design**

Publisher: ACM Press

Full text available: pdf(271.92 KB) Additional Information: full citation, references, citings, index terms

13 Contest: a concurrent test generator for sequential circuits

Vishwani D. Agrawal, Kwang-Ting Cheng, Prathima Agrawal

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Publisher: IEEE Computer Society Press

Full text available: pdf(764.79 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes the application of a concurrent fault simulator to automatic test vector generation. As faults are simulated in the fault simulator a cost function is simultaneously computed. A simple cost function is the distance (in terms of the number of gates and flip-flops) of a fault effect from a primary output. The input vector is then modified to reduce the cost function until a test is found. The paper presents experimental results showing the effectiveness of this method in ...

14 Methods for encrypting and decrypting MPEG video data efficiently

Lei Tang

February 1997 **Proceedings of the fourth ACM international conference on Multimedia**

Publisher: ACM Press

Full text available: pdf(1.45 MB) Additional Information: full citation, references, citings, index terms

Keywords: MPEG codec, compression, multimedia commerce, multimedia encryption, multimedia security

15 Physical Design: EVE: a CAD tool for manual placement and pipelining assistance of FPGA circuits

William Chow, Jonathan Rose

February 2002 **Proceedings of the 2002 ACM/SIGDA tenth international symposium on Field-programmable gate arrays**

Publisher: ACM Press

Full text available: pdf(352.87 KB) Additional Information: full citation, abstract, references, citings

As FPGAs push ever deeper into mainstream digital design, there is an increasing desire for high-performance circuits. This paper describes a manual editor, called EVE, which can assist a designer to perform manual packing, placement and pipelining of commercial FPGA circuits to achieve a meaningful increase in performance. This effort is inspired by Von Herzen's paper [15] [16], which proposed the notion of an "Event Horizon" - a high-speed circuit design approach in which complete knowledge of ...

Keywords: FPGA, event horizon, manual placement and pipelining, programmable logic

16 Mixed-signal design and simulation: A 16-bit mixed-signal microsystem with integrated CMOS-MEMS clock reference

Robert M. Senger, Eric D. Marsman, Michael S. McCorquodale, Fadi H. Gebara, Keith L. Kraver, Matthew R. Guthaus, Richard B. Brown

June 2003 **Proceedings of the 40th conference on Design automation**

Publisher: ACM Press

Full text available: pdf(793.60 KB) Additional Information: full citation, abstract, references, citings, index terms

In this work, we report on an unprecedented design where digital, analog, and MEMS technologies are combined to realize a general-purpose single-chip CMOS microsystem. The convergence of these technologies has enabled the development of a low power, portable microinstrument ideally suited for controlling environmental and bio-implantable sensors.

Keywords: ADC, MEMS, PGA, SD, SoC, clock generation, design methodology, inductor, low power, low voltage analog, microcontroller, microsystem, mixed-signal, system-on-chip, varactor

17 Fortran 8X draft

Loren P. Meissner

December 1989 **ACM SIGPLAN Fortran Forum**, Volume 8 Issue 4

Publisher: ACM Press

Full text available: pdf(21.36 MB) Additional Information: full citation, abstract, index terms

Standard Programming Language Fortran. This standard specifies the form and establishes the interpretation of programs expressed in the Fortran language. It consists of the specification of the language Fortran. No subsets are specified in this standard. The previous standard, commonly known as "FORTRAN 77", is entirely contained within this standard, known as "Fortran 8x". Therefore, any standard-conforming FORTRAN 77 program is standard conforming under this standard. New features can b ...

18 A low-power clock and data recovery circuit for 2.5 Gb/s SDH receivers

Andrea Pallotta, Francesco Centurelli, Alessandro Trifiletti
August 2000 **Proceedings of the 2000 international symposium on Low power electronics and design**
Publisher: ACM Press
Full text available: pdf(637.65 KB) Additional Information: full citation, abstract, references, index terms

A low power monolithic Clock and Data Recovery IC for 2.5 Gb/s SDH STM-16 systems has been designed and fabricated using Maxim GST-2 27 GHz-fT Silicon bipolar technology. The circuit performs the following functions: signal amplification and limitation, clock recovery and decision; a single 3.3 V supply voltage is required, and power consumption results below 350 mW. This IC and a previously presented transimpedance amplifier so allows composing a chip set for the recei ...

Keywords: SDH, clock recovery, low power, optical communications

19 A digital system modeling philosophy and design language

Mehmet B. Baray, Stephen Y. H. Su
June 1971 **Proceedings of the 8th workshop on Design automation**
Publisher: ACM Press
Full text available: pdf(1.13 MB) Additional Information: full citation, abstract, references, citings, index terms

With the increasing complexity of digital systems, a new approach to system decomposition and modelling must be developed. Such an approach must not only permit a system to be described in a modular fashion, but the basic system modules must be able to be decomposed to allow a precise description of the module function. In this paper, a modelling philosophy and language are presented which permit the system designer to: (1) specify the system design in a hierarchical, modular fashion; (2) d ...

20 Two-dimensional position deteciton system with MEMS accelerometer for MOUSE applications

Seungbae Lee, Gi-Joon Nam, Junseok Chae, Hanseup Kim, Alan J. Drake
June 2001 **Proceedings of the 38th conference on Design automation**
Publisher: ACM Press
Full text available: pdf(1.40 MB) Additional Information: full citation, abstract, references, index terms

A hybrid two-dimensional position sensing system is designed for mouse applications. The system measures the acceleration of hand-movements which are converted into two-dimensional location coor-dinates. The system consists of four major components: 1) MEMS accelerometers, 2) CMOS analog read-out circuitry, 3) an accelera-tion magnitude extraction module, and 4) a 16-bit RISC micropro-cessor. Mechanical and analog circuit simulation shows that the designed padless mouse system can detect a ...

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Zheng, L.; Yoshikawa, N.; Deng, J.; Meng, X.; Whiteley, S.; van Duzer, T.;
Applied Superconductivity, IEEE Transactions on
Volume 9, Issue 2, Part 3, June 1999 Page(s):3310 - 3313
Digital Object Identifier 10.1109/77.783737
AbstractPlus | References | Full Text: PDF(516 KB) **IEEE JNL**

2. **A 4-bit Josephson data processor chip**
Hatano, Y.; Yano, S.; Mori, H.; Yamada, H.; Hirano, M.; Kawabe, U.;
Solid-State Circuits, IEEE Journal of
Volume 24, Issue 5, Oct 1989 Page(s):1312 - 1316
Digital Object Identifier 10.1109/JSSC.1989.572605
AbstractPlus | Full Text: PDF(768 KB) **IEEE JNL**

3. **Single flux, quantum B flip-flop and its possible applications**
Polonsky, S.V.; Semenov, V.K.; Kirichenko, A.F.;
Applied Superconductivity, IEEE Transactions on
Volume 4, Issue 1, March 1994 Page(s):9 - 18
Digital Object Identifier 10.1109/77.273059
AbstractPlus | Full Text: PDF(724 KB) **IEEE JNL**

4. **9 K operation of RSFQ logic cells fabricated by NbN integrated circuit tec**
Terai, H.; Wang, Z.;
Applied Superconductivity, IEEE Transactions on
Volume 11, Issue 1, Part 1, March 2001 Page(s):525 - 528
Digital Object Identifier 10.1109/77.919398
AbstractPlus | References | Full Text: PDF(500 KB) **IEEE JNL**

5. **Dc-free convolutional codes and dc-free turbo codes**
Fengqin Zhai; Yan Xin; Fair, I.J.;
Communications, 2005. ICC 2005. 2005 IEEE International Conference on
Volume 1, 16-20 May 2005 Page(s):632 - 636 Vol. 1
Digital Object Identifier 10.1109/ICC.2005.1494428
AbstractPlus | Full Text: PDF(310 KB) **IEEE CNF**

6. **GaAs MESFET logic with 4-GHz clock rate**
Van Tuyl, R.L.; Liechti, C.A.; Lee, R.E.; Gowen, E.;

Solid-State Circuits, IEEE Journal of
Volume 12, Issue 5, Oct 1977 Page(s):485 - 496
AbstractPlus | Full Text: PDF(1584 KB) IEEE JNL

☐ 7. **RSFQ arithmetic blocks for DSP applications**
Polonsky, S.V.; Jao Ching Lin; Rylyakov, A.V.;
Applied Superconductivity, IEEE Transactions on
Volume 5, Issue 2, Part 3, Jun 1995 Page(s):2823 - 2826
Digital Object Identifier 10.1109/77.403179
AbstractPlus | Full Text: PDF(368 KB) IEEE JNL

☐ 8. **4-bit rapid single-flux-quantum decoder**
Kirichenko, A.F.; Semenov, V.K.; Kwong, Y.K.; Nandakumar, V.;
Applied Superconductivity, IEEE Transactions on
Volume 5, Issue 2, Part 3, Jun 1995 Page(s):2857 - 2860
Digital Object Identifier 10.1109/77.403187
AbstractPlus | Full Text: PDF(312 KB) IEEE JNL

☐ 9. **A DC-powered Josephson logic family that uses hybrid unlatching flip-flc elements (Huffles)**
Hasegawa, H.; Nagaishi, H.; Kominami, S.; Yamada, H.; Nishino, T.;
Applied Superconductivity, IEEE Transactions on
Volume 5, Issue 4, Dec. 1995 Page(s):3504 - 3510
Digital Object Identifier 10.1109/77.482141
AbstractPlus | Full Text: PDF(648 KB) IEEE JNL

☐ 10. **Josephson counting analog-to-digital converter**
Miller, D.L.; Przybysz, J.X.; Kang, J.; Hamilton, C.A.; Burnell, D.M.;
Magnetics, IEEE Transactions on
Volume 27, Issue 2, Part 4, Mar 1991 Page(s):2761 - 2764
Digital Object Identifier 10.1109/20.133783
AbstractPlus | Full Text: PDF(304 KB) IEEE JNL

☐ 11. **A 1-GHz-clock Josephson microcomputer system**
Yano, S.; Hatano, Y.; Mori, H.; Yamada, H.; Nakahara, K.; Hirano, M.; Kawabe
Magnetics, IEEE Transactions on
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Digital Object Identifier 10.1109/20.133750
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☐ 12. **A voltage compensated series-gate bipolar circuit operating at sub-2 V**
Sato, H.; Ueda, K.; Sasaki, N.; Ikeda, T.; Mashiko, K.;
Solid-State Circuits, IEEE Journal of
Volume 29, Issue 10, Oct. 1994 Page(s):1200 - 1205
Digital Object Identifier 10.1109/4.315203
AbstractPlus | Full Text: PDF(460 KB) IEEE JNL

☐ 13. **8-channel×2.5 Gbit/s hybrid integrated multiwavelength photoreceiver m arrayed-waveguide grating demultiplexer**
Ohyama, T.; Akahori, Y.; Yamada, T.; Ishii, M.; Kamei, S.; Sakai, Y.;
Electronics Letters
Volume 38, Issue 9, 25 April 2002 Page(s):419 - 421
Digital Object Identifier 10.1049/el:20020296
AbstractPlus | Full Text: PDF(436 KB) IEE JNL

☐ 14. **Resolution enhancement and dither of sigma-delta modulator digital-to-a converters**
Magrath, A.J.; Sandler, M.B.;

Electronics Letters
Volume 31, Issue 18, 31 Aug. 1995 Page(s):1540 - 1542
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